

What is claimed is:

1     Claim 1. In an SMP computer system having an  
2     source-synchronous pipelined, self-calibrating interface,  
3     the method of recalibrating the interface, comprising the  
4     steps of:  
5       a) halting operations of said SMP computer system having an  
6       source-synchronous pipelined, self-calibrating interface to  
7       idle the interface,  
8       b) fencing the interface,  
9       c) recalibrating the interface using clock readjustment,  
10      d) unfencing the interface, and  
11      e) commencing operations to allow interface use again.

1     Claim 2. The method according to claim 1, wherein said step  
2     of halting operations is done with a system quiesce  
3     operation.

1     Claim 3. The method according to claim 1, wherein said step  
2     of calibrating the interface is accomplished by sampling a  
3     known data pattern.

1     Claim 4. The method according to claim 1, wherein said step  
2     of calibrating the interface is accomplished by  
3     recalculating the frequency and applying the appropriate  
4     delay adjustment to the clock.

1     Claim 5. In an SMP computer system having an  
2     source-synchronous interface, the method for re-calibration  
3     of the interface at periodic intervals comprising the steps  
4     of:  
5       a. putting the system of the interface into a wait state,  
6       b. performing a fast initialization process for calibration,  
7       c. taking the system of the interface out of said wait  
8     state.

1      Claim 6. The method according to claim 5 wherein a  
2      step of data deskew has been performed as part of the  
3      original system interface initialization, and during  
4      recalibration of only a single clock centering step for the  
5      interface is performed during said fast initialization  
6      process for calibration without deskewing data during said  
7      fast initialization step performed for re-calibration.

1      Claim 7. The method according to claim 6 wherein said wait  
2      state keeps the interface from being used for processing  
3      steps other than re-calibration and sending a calibration  
4      pattern and allowing calibration logic to re-center the  
5      clock applicable to the interface to compensate for new  
6      environmental conditions and circuit changes.

1      Claim 8. The method according to claim 7 wherein the  
2      recalibration of the interface is triggered periodically and  
3      in a manner that circuit or environmental characteristics  
4      over time do not adversely affect the operation of the  
5      interface.

1      Claim 9. The method according to claim 7 wherein the  
2      re-calibration is based on a trigger event which triggers  
3      the steps for re-calibration of the interface

1      Claim 10. The method according to claim 1 wherein a quiesce  
2      of the system of the interface is performed prior to  
3      performing a fast initialization process for calibration,  
4      and during calibration, the step of calibrating the  
5      interface recalculates the frequency of the clock for the  
6      interface and applies an appropriate delay adjustment to the  
7      clock for the interface, after which the system for the

8       interface is unquiesced before commencing operations to  
9       allow interface use again.

1       Claim 11. The method according to claim 10 wherein the  
2       recalibration stem includes sending a pattern across the  
3       interface and adjusting the clock through re-centering  
4       without data de-skewing but with shifing to the clock to  
5       re-center the intrface data capturing window for the 'eye'  
6       of the data capturing window.

1       Claim 12. The method according to claim 10 wherein the  
2       recalibration stem includes re-calculating the clock  
3       frequency of the interface against the current hardware and  
4       re-applying the clock frequency calculation to the clock  
5       delay to re-center the clock when the machine is being  
6       cycled down to failure and the major change needing  
7       re-calibration is cycle time.

1       Claim 13. The method of claim 5 wherein a state machine  
2       controls calibration, and said state machine allows  
3       a. putting the system of the interface into a wait state and  
4       for quiescing the data over the interface when the state  
5       machine enters a re-calibration state, whereupon,  
6       b. said a fast initialization process for calibration is  
7       performed, and then  
8       c. a change of said stae machine changes the system of the  
9       interface back out of said wait state; and  
10      d. Allows data to transfer across the interface again.